

$F / G. 2$

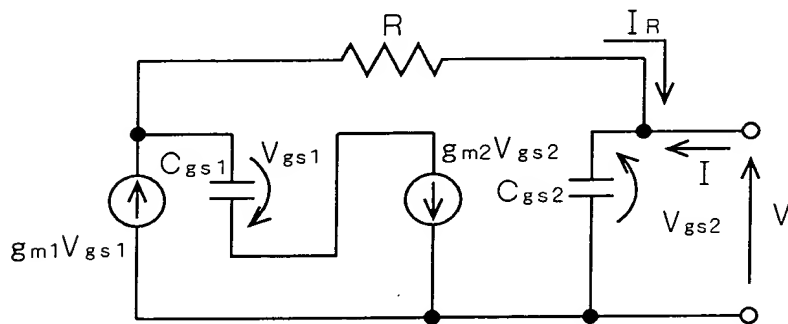


FIG. 4

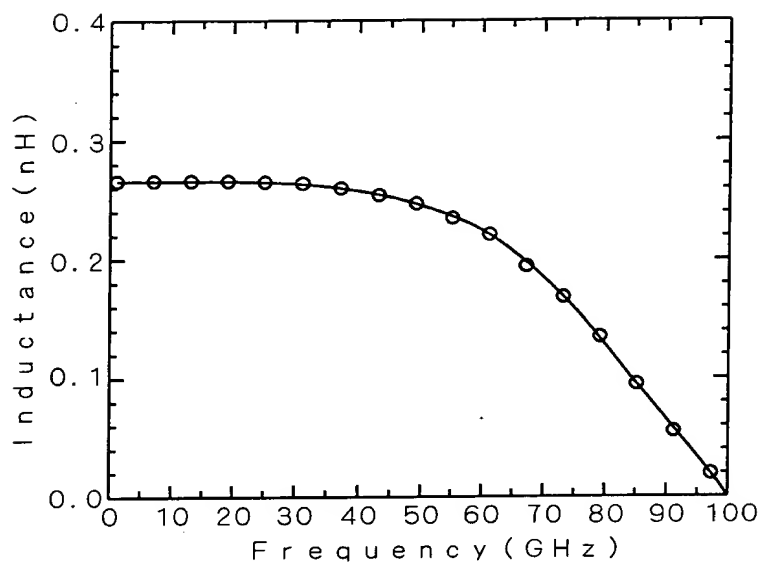


FIG. 5

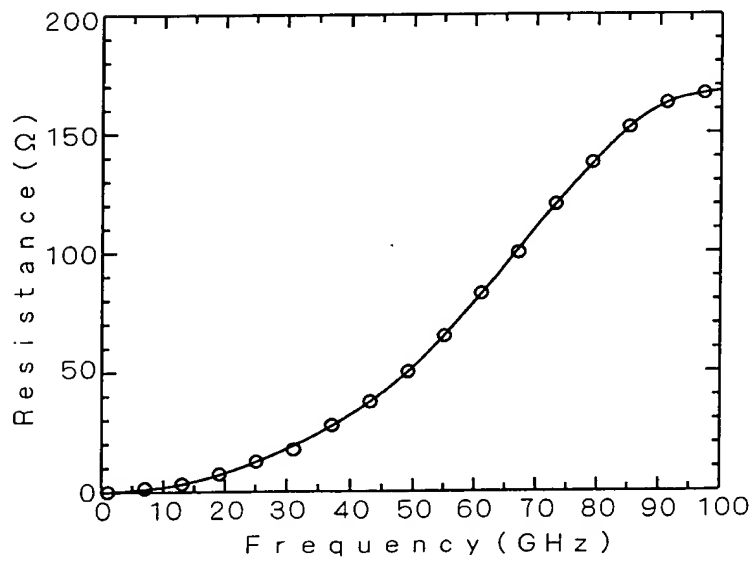


FIG. 6

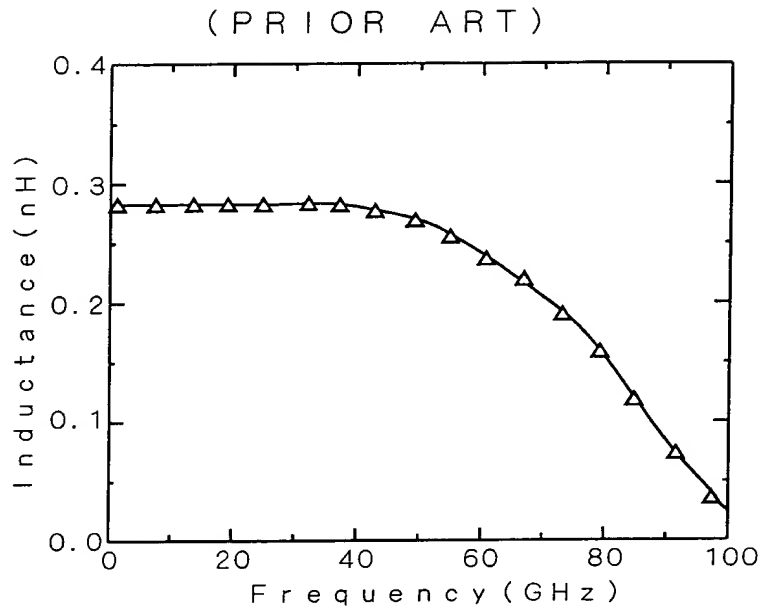
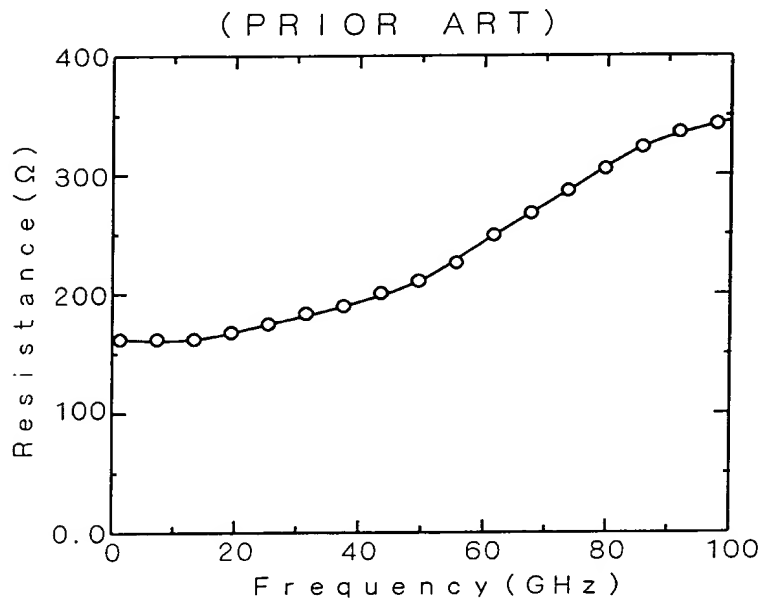


FIG. 7



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

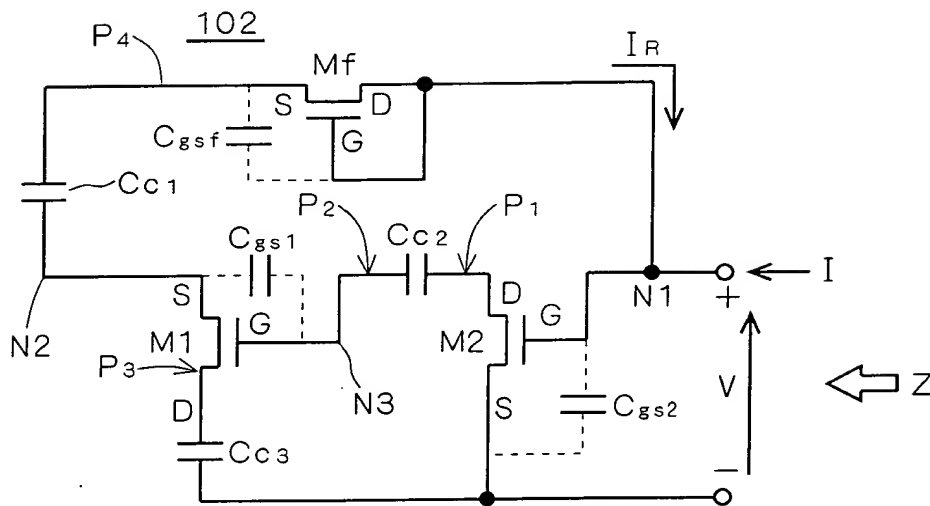


FIG. 10

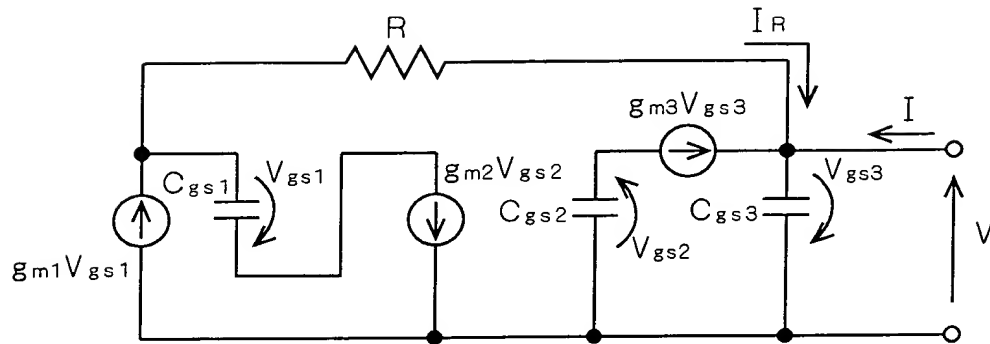


FIG. 11

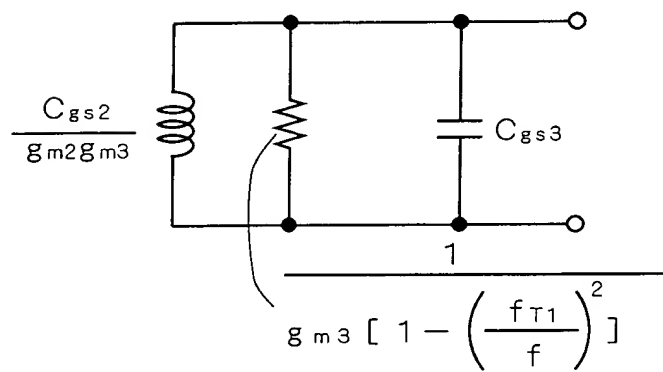


FIG. 12

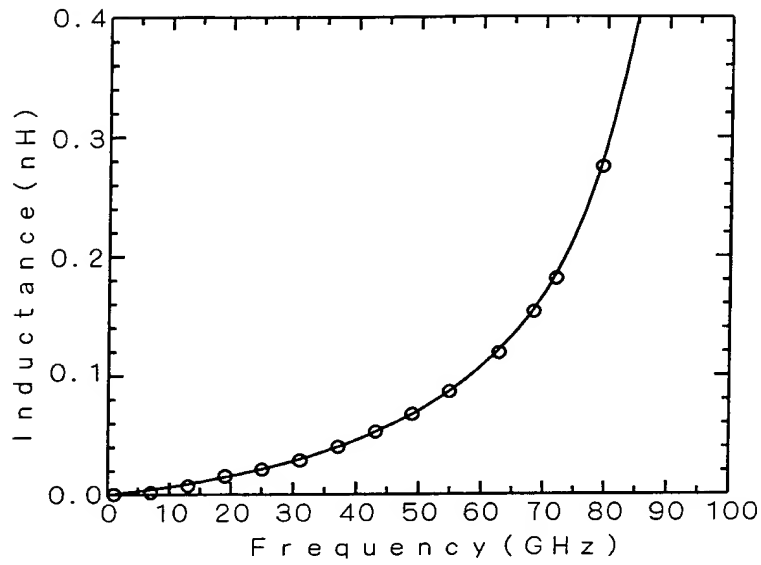


FIG. 13

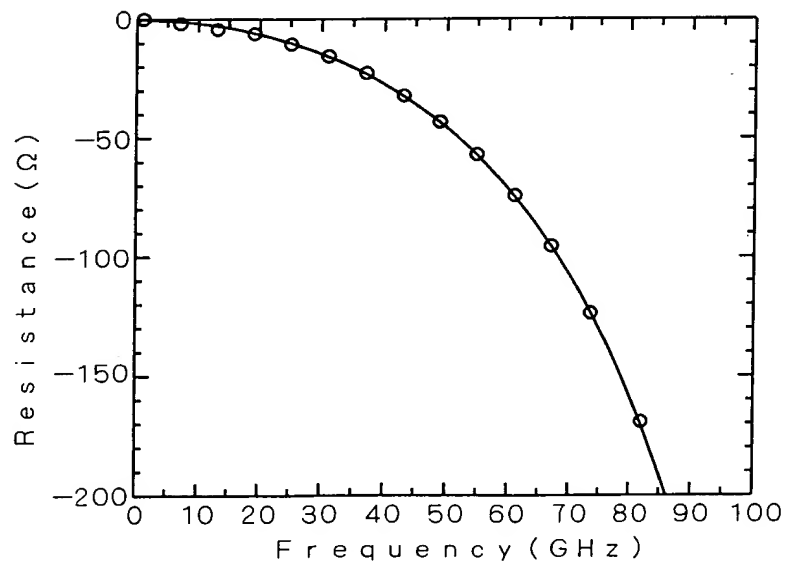
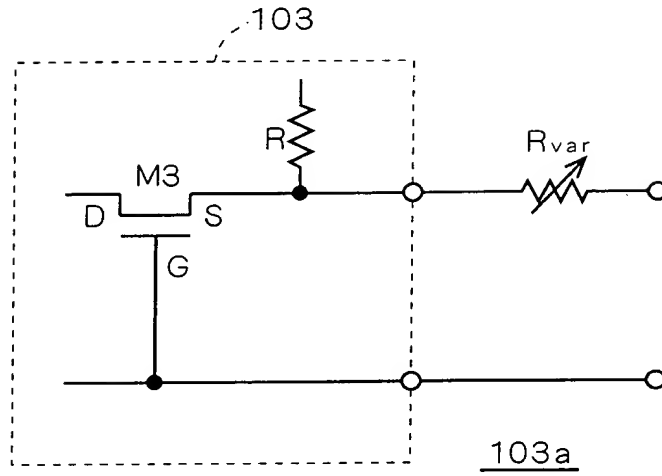


FIG. 14



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The circuit diagram shows a differential amplifier with current mirrors and cascode stages. The input stage consists of a differential pair of NMOS transistors, M1 and M2, with gates connected to a common-mode bias voltage V_{CM} . The sources of M1 and M2 are connected to a common source node, which is biased by a current source I_{SS} connected to ground. The drains of M1 and M2 are connected to a differential load consisting of a resistor R and a capacitor C_{c1} in parallel. The output of the first stage is taken from the drain of M1. The second stage is a cascode stage consisting of a PMOS transistor M3 and an NMOS transistor M4. The gate of M3 is connected to a bias voltage V , and its source is connected to the drain of M2. The gate of M4 is connected to a bias voltage V , and its source is connected to the drain of M1. The drain of M3 is connected to a current source I_{SS} and a load capacitor C_{c2} . The drain of M4 is connected to a current source I_{SS} and a load capacitor C_{c3} . The output of the second stage is taken from the drain of M4. The circuit is biased by a common-mode bias voltage V_{CM} and a differential-mode bias voltage V . The load capacitors are labeled C_{c1} , C_{c2} , and C_{c3} . The transistors are labeled M1, M2, M3, and M4. The current sources are labeled I_{SS} and I_{SS} . The resistor is labeled R . The bias voltages are labeled V_{CM} and V . The output is labeled V .

FIG. 16

FIG. 16

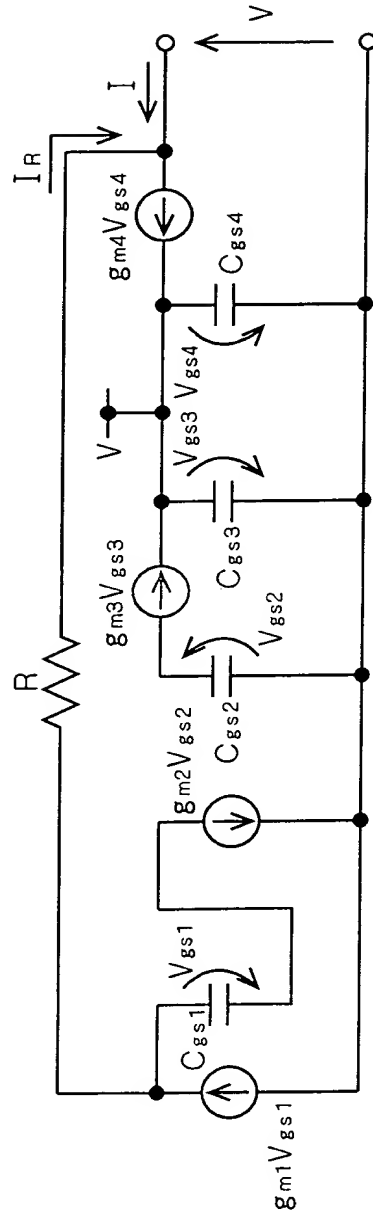


FIG. 17

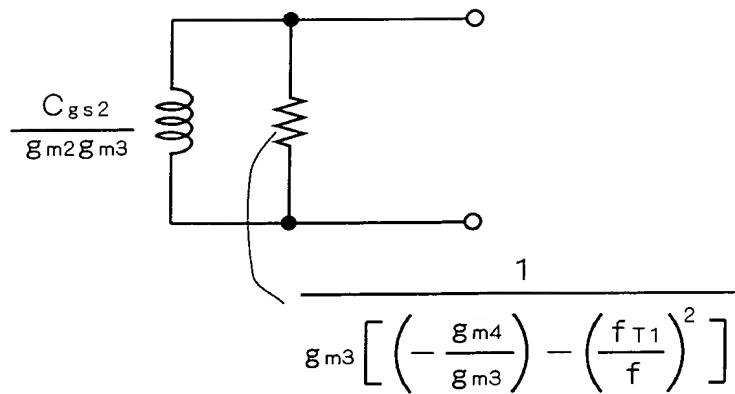


FIG. 18

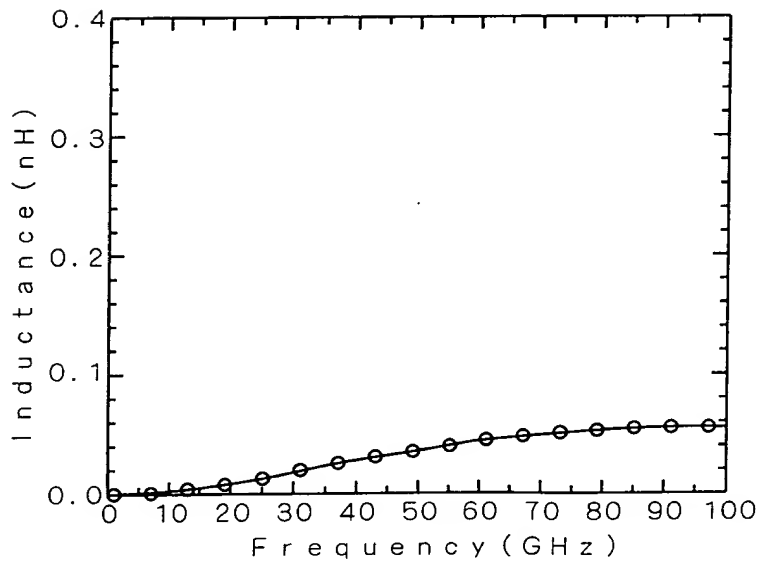


FIG. 19

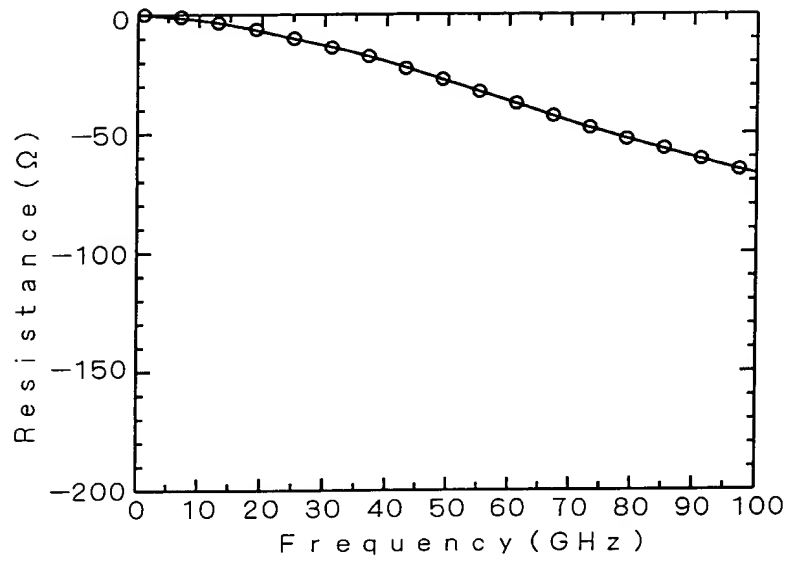


FIG. 20

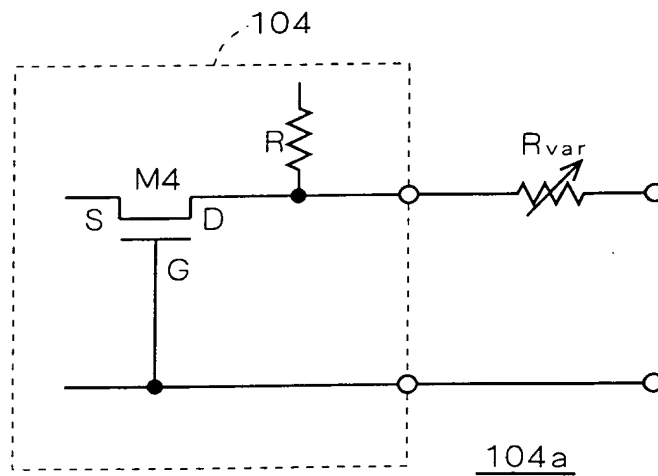


FIG. 21

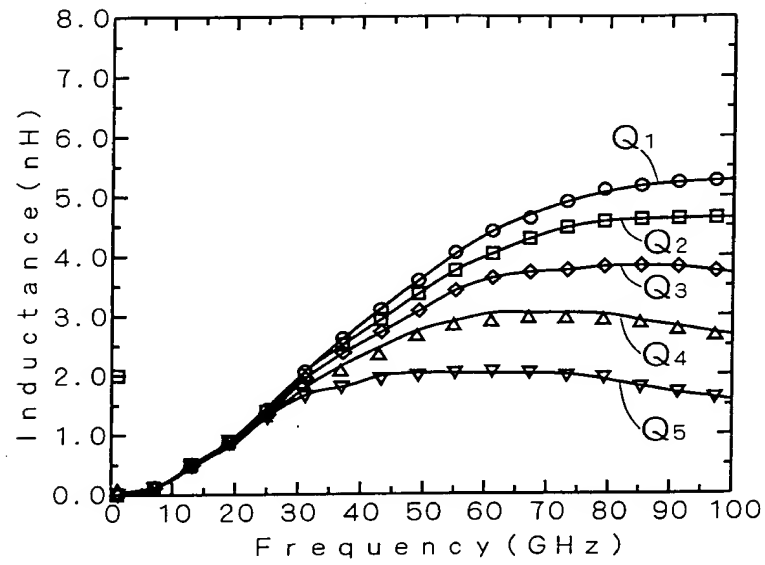


FIG. 22

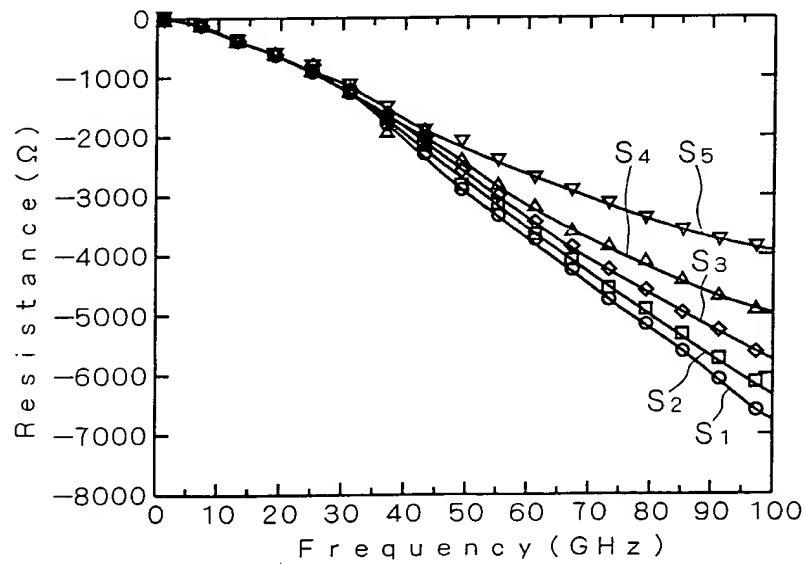


FIG. 23

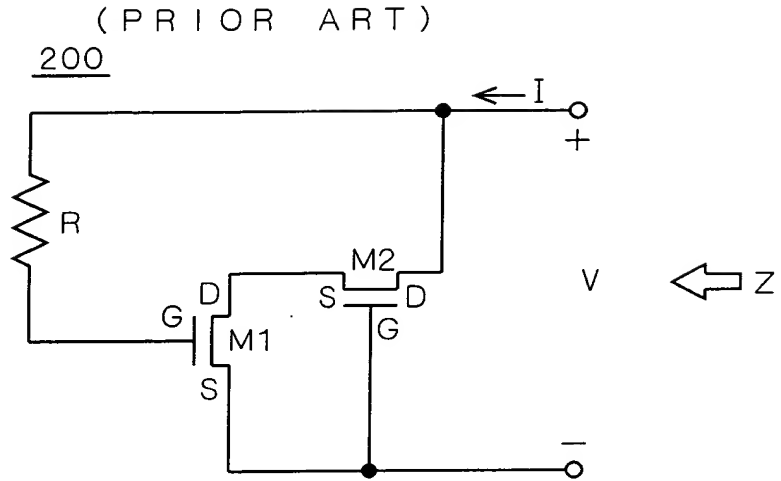


FIG. 24

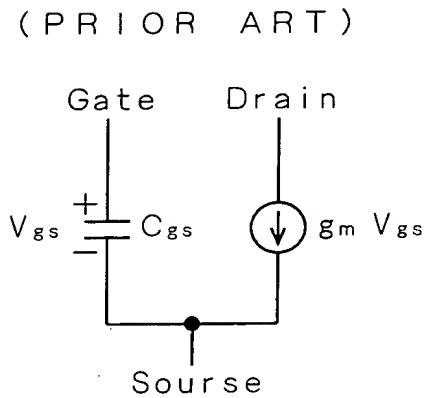


FIG. 25

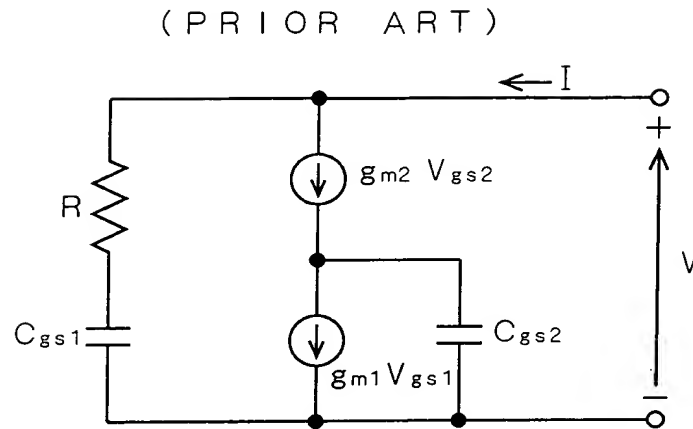


FIG. 26

